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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,229	01/26/2001	Takanori Iwamatsu	FUJS 13.045A	6938

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EXAMINER
TSE, YOUNG TOI

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,229	IWAMATSU ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Reissue Applications

1. The reissue oath/declaration filed with this application is defective because it fails to contain the statement required under 37 CFR 1.175(a)(1) as to applicant's belief that the original patent is wholly or partly inoperative or invalid. See 37 CFR 1.175(a)(1) and see MPEP § 1414.

Applicants belief that an error has been made by reason of the patentees claiming less than they had the right to claim in the patent. In particular, the patentees concluded that a generic claim could have been included among the claims during prosecution of the elected species.

Had a generic claim been entered and allowed in the parent case, then following allowance of the elected claims, the examiner would have examined a reasonable number of additional species. Failure to have additional species examined in the parent case was the penalty paid for the error of omitting a generic claim. The reissue application has the objective of rectifying that error and defining a generic claim and thereby also cover hopefully all species that were originally claimed in the parent application.

The generic claim 47 has been added and is intended to relate to each other of the six embodiments. The preamble to claim 47 states: "A receiver circuit arranged in a receiving unit of multiplex radio equipment ...."

The allowed claim 1 is changed in the preamble from "A clock phase detecting circuit arranged in a receiving unit of multiplex radio equipment" to -- A receiver

arranged in a receiver unit of multiplex radio equipment --. Each of the other claims 2-26 has the identical opening language or has been amended to have the identical language to emphasize a generic relationship between the 47 claims.

However, according to MPEP 1450 Restriction and Election of Species. A reissue applicant's failure to timely file a divisional application is not considered to be the error causing a patent granted on elected claims to be partially inoperative by reason of claiming less than the applicant had a right to claim. Thus, such error is not correctable by reissue of the original patent under 35 U.S.C. 251. In re Watkinson, 900 F.2d 230, 14 USPQ2d 1407 (Fed. Cir. 1990); In re Orita, 550 F.2d 1277, 1280, 193 USPQ 145, 148 (CCPA 1997). See also In re Mead, 581 F. 2d 251, 198 USPQ 412 (CCPA 1978). Likewise, if the original patent specification or the prosecution history of the original patent shows an intent not to claim the newly presented invention, that invention cannot be added by reissue.

2. Claims 1-47 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference sign "307" is not shown in Fig. 14 as mentioned on column

26, line 34. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: column 2, line 12, "A/ID" should be changed to – A/D – and line 48, "a infinite phase shift" should be changed to -- an infinite phase shifter --; column 4 (line 23 and line 60), column 6 (line 14), the semicolon ":" should be deleted; column 14, line 1, "14" should be changed to –14A --; column 25, line 58, "27" should be changed to -- 27A --, line 61, "27" should be changed to – 27B --, line 62, "A/ID" should be changed to – A/D --; column 26, line 42, "FE" should be changed to – FF --; and column 34, line 53, "A/ID" should be changed to – A/D --. Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 3-28, 30-32, 34-39, and 41-46 are objected to because of the following informalities: in claim 8, lines 20-21, "an input signal to output signal error" appears to read – the input signal and the output signal --; in claim 14, line 7, "said specific signal

judging unit" should be changed to – said plural signal judging units --; in claim 15, line 20, "input/output signals" should be changed to – the input signal and the output signal --; dependent claims 16-21, 23-28, 30-32, 34-39, and 41-46 are not consisted with dependent claims 3-7 and 9-14, for example, dependent claims 3-7 and 9-14 start with "A receiver circuit …", but dependent claims 16-21, 23-28, 30-32, 34-39, and 41-46 start with "The receiver circuit …"; in claim 22, lines 7-8, the phrase "by demodulating a multilevel orthogonal modulated signal and an equalization circuit" should be changed to -- by demodulating the multilevel orthogonal modulated signal --, line 15, "signals input to or output from" should be changed to – the input signal and the output signal from --, line 18, "a signal" should be changed to – the signal --, and lines 20-21, "the output from" should be changed to –from the output of --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 16-21, 23-28, 34-39, and 41-46 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The configuration or some of the claimed subject matter does not correspond to the disclosure of the drawings.

According to the present invention, Fig. 1 shows a first embodiment of a clock phase detecting circuit, wherein Figs. 7-27 show the detailed embodiments of the clock phase detecting circuit of Fig. 1 as recited in claims 1-14; Fig. 2 shows a second embodiment of a clock phase detecting circuit, wherein Figs. 28-42 show the detailed embodiments of the clock phase detecting circuit of Fig. 2 as recited in claims 15-21; Fig. 3 shows a third embodiment of a clock phase detecting circuit, wherein Figs. 43-50 show the detailed embodiments of the clock phase detecting circuit of Fig. 3 as recited in claims 22-28; Fig. 4 shows a fourth embodiment of a clock phase detecting circuit, wherein Figs. 51-59 show the detailed embodiments of the clock phase detecting circuit of Fig. 4 as recited in claims 29-32; Fig. 5 shows a fifth embodiment of a clock phase detecting circuit as recited in claims 33-39; and Fig. 6 shows a sixth embodiment of a clock phase detecting circuit as recited in claims 40-46.

Clearly, no single figure or combination of circuits includes all the claimed subject matter of the average unit, the plurality of identifying circuit, the plurality of phase adjusting units, the plurality of clock phase detecting units, the selecting unit, and the composing unite as recited in *claims* 16-21, 23-28, 34-39, and 41-46.

9. Claims 19, 24-27, 29-39, and 43-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19 (line 9), claim 24 (lines 6-7), claim 25 (lines 12 and 14), claim 29 (line 15), claim 31 (lines 3, 4-5, and 5-6), claim 32 (lines 3, 5, and 5-6), claim 33 (lines 14 and 20-21), claim 38 (lines 12-13), and claim 43 (line 12), the phrases "wherein plural phase adjusting units and plural clock phase detecting units", "wherein plural clock phase detecting units", "said phase adjusting unit", "said resultant phase component", "said clock phase calculating unit", "said error detecting unit", "said signal inclination detecting unit", "the resultant clock", and "said averaging units and said clock phase detecting units" all lack antecedent basis.

In line 11 of claims 26-27 and 44-45, the phrase "a method different from ..." is vague and indefinite because it is unclear what is used in the method.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 29-32, 40-42, 44, and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Onoda et al. (newly cited).

Onoda et al. (U.S. Patent No. 5,317,602) discloses an orthogonal or QPSK receiver in Fig. 5 including mixers (51 and 52) for mixing an IF signal with a local oscillator signal generated by a local oscillator (53); filters (55 and 56) for filtering the mixed signals; A/D converters (57 and 58) for converting the filtered signals into digital signals; an operation circuit (59), and discriminators (60 and 61) for converting the digital signals into an in-phase (I) signal and a quadrature-phase (Q) signal; a P/S converter (62) for converting the quadrature signals into a serial signal; and a bit time recovery circuit (1) for providing clock signals to the A/D converters (57 and 58), the operation circuit (59), the discriminators (60 and 61), and the P/S converter (62).

The bit time recovery circuit (1) includes a phase comparison result detection unit (2) and a digital PLL unit (3). The phase comparison result detection unit (2) comprises flip-flops FFs (21 and 22) and Exclusive OR circuits (23 and 24) for providing a comparison signal. The digital PLL unit (3) comprises a sequential filter (35), an oscillator (31), a pulse control circuit (32), a first divider (33), and a second divider (34) for generating clock signals.

With respect to claim 29, the A/D converters (57 and 58) along or the combination of the mixers (51 and 52), the filters (55 and 56), the operation circuit (59), the discriminators (60 and 61), and the P/S converter (62) correspond to the identifying

circuit for identifying the IF signal; the phase comparison result detection unit (2) along or the bit time recovery circuit (1) except the divider (34) corresponds to the clock phase detecting unit for detecting a phase component of the digital signals generated from the A/D converters (57 and 58) and the clock signal provided by the divider (34); and the digital PLL unit (3) or the divider (34) correspond to the clock regenerating circuit for generating the clock signal to both the A/D converters (57 and 58) and the phase comparison result detection unit (2).

With respect to claim 30, one of the FFs (21 and 22) corresponds to the clock phase difference detecting unit, one of the FFs (21 and 22) corresponds to the signal error differential detecting unit, and one or both of the Exclusive OR circuits (23 and 24) corresponds to the clock phase calculating unit.

With respect to claim 31, two dividers (33 and 34) are shown within the digital PLL unit (3).

With respect to claim 32, two Exclusive OR circuits (23 and 24) are shown within the phase comparison result detection unit (2).

With respect to claim 40, the A/D converters (57 and 58) along or the combination of the mixers (51 and 52), the filters (55 and 56), the operation circuit (59), the discriminators (60 and 61), and the P/S converter (62) correspond to the identifying circuit for identifying the IF signal; the bit time recovery circuit (1) corresponds to the clock regenerating circuit, which comprises the phase comparison result detection unit (2) and the digital PLL unit (3); the phase comparison result detection unit (2) corresponds to the clock phase detecting unit; the filter (35) corresponds to the loop

filter unit; and the oscillator (31), the pulse control (32), and the dividers (33 and 34) correspond to the oscillator unit.

With respect to claims 41 and 42, the A/D converters (57 and 58) are located in two separated channels. Therefore, each of the A/D converters (57 and 58) corresponds to one identifying circuit.

With respect to claim 44, one of the FFs (21 and 22) corresponds to the first clock phase detecting unit, one of the FFs (21 and 22) corresponds to the second clock phase detecting unit, and one or both of the Exclusive OR circuits (23 and 24) corresponds to the composing unit.

With respect to claim 47, it is a generic claim, which includes the claimed limitations of two different parts, wherein one part has the similar claimed subject matter of claim 40.

12. Claims 33, 35, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Oie et al. (newly cited).

Oie et al. (U.S. Patent No. 5,438,591) discloses a demodulation circuit in Fig. 2 including mixers (2a and 2b) for mixing an IF signal (1) with a local oscillator signal generated by a local oscillator (9); a clock reproducing circuit (3) for providing clock signals; an identifying unit (4) or A/D converters (4a and 4b) for converting the mixed signals into digital signals; a phase difference signal detection circuit (12) for detecting the digital signals; a demodulation logic circuit (5); a digital logical processing circuit (6); an abnormal synchronization preventing circuit (13); a data selector (7); an amplifier (8); and a phase shifter (10).

With respect to claim 33, the identifying unit (4) or A/D converters (4a and 4b) corresponds to the identifying circuit for identifying the IF signal; the clock reproducing circuit (3) corresponds to the clock regenerating unit and the phase adjusting unit for providing a clock phase difference information to the identifying unit (4) or A/D converters (4a and 4b); and the phase difference signal detection circuit (12) corresponds to the clock phase detecting unit for detecting the clock phase difference information and a signal error differential information from the identifying unit (4) or A/D converters (4a and 4b).

With respect to claims 35 and 37, the A/D converters (4a and 4b) are located in two separated channels. Therefore, each of the A/D converters (4a and 4b) corresponds to one identifying circuit, wherein the clock reproducing circuit (3) and the phase difference signal detection circuit (12) are used in common to the A/D converters (4a and 4b).

13. Claims 29-30, 40-42, and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (previously cited).

Kobayashi (U.S. Patent No. 5,535,252) discloses a clock synchronization circuit in Fig. 2 for use in a base-band demodulator of communication equipment of a digital modulation type.

In Fig. 2, the base-band demodulator (4) comprises A/D converters (41 and 42) for converting analog signals (a and b) into digital signals (c and d); a delay detector (43) for detecting the digital signals to provide detected signals (e and f); a judger circuit (44) for judging the detected signals to provide a judged signal (g); a PLL (40) for

providing clock signals; a limiter (45); a band pass filter (46); a phase error detector (47); a clock reproducer (48); and a frequency divider (49).

With respect to claim 29, the A/D converters (41 and 42) correspond to the identifying circuit for identifying the IF signals (a and b); the phase error detector (47) corresponds to the clock phase detecting unit for detecting a phase component of the digital signals generated from the A/D converters (41 and 42); and the clock reproducer (48) corresponds to the clock regenerating circuit for generating the clock signal to both the A/D converters (41 and 42) and the phase error detector (47).

With respect to claim 30, the detailed embodiment of the phase error detector (47) is shown in Fig. 8, wherein the delay circuit (471) and the sign comparator (472) correspond to the clock phase difference detecting unit; the counter (473) corresponds to the signal error differential detecting unit; and the judger circuit (474) corresponds to the clock phase calculating unit.

With respect to claim 40, the A/D converters (41 and 42) corresponds to the identifying circuit for identifying the IF signal (a and b); the PLL (40) and the reproducer (48) correspond to the loop filter unit and the oscillating unit (note it is well known in the art that the PLL 40 includes at least a loop filter and an oscillator); and the clock reproducer (48) corresponds to the clock phase detecting unit.

With respect to claims 41 and 42, the A/D converters (41 and 42) are located in two separated channels. Therefore, each of the A/D converters (41 and 42) corresponds to one identifying circuit.

With respect to claim 47, it is a generic claim, which includes the claimed limitations of two different parts, wherein one part has the similar claimed subject matter of claim 40.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Kanzaki (U.S. Patent No. 5,579,346), Becher et al. (U.S. Patent No. 5,612,975), and Gotoh (U.S. Patent No. 5,656,971) are related to a phase demodulator circuit having a carrier phase synchronization circuit for providing a controlled clock signal to an identifying circuit of the phase demodulator circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

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Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
2/20/03